

I CLAIM:

1 1. A post-processing method for use in a sampled data read channel
2 of a mass data storage device that has a Viterbi detector that
3 receives actual sampled partial response target data from a said
4 data medium of a mass data storage device and produces a recovered
5 data output signal, comprising:

6 filtering an a recovered partial response target signal
7 derived from said recovered data output signal and said sampled
8 partial response target data to produce a filtered output signal;

9 providing a threshold circuit to provide a threshold against
10 which said filtered output signal is compared;

11 generating an error event pattern indicating signal when a
12 predetermined error event pattern occurs in said recovered data
13 output signal;

14 and modifying the recovered data output signal when said
15 filtered output signal exceeds the threshold of said threshold
16 circuit and said error event indicating signal is generated.

1 2. The method of claim 1 wherein said Viterbi detector is an EEPR4
2 Viterbi detector.

1 3. The method of claim 1 wherein said Viterbi detector is an EEPR4
2 Viterbi detector.

1 4. The method of claim 1 wherein said error event pattern is $ex =$
2 $\pm\{1\}$.

1 5. The method of claim 1 wherein said error event pattern is $ex =$
2 $\pm\{1-11\}$.

1 6. The method of claim 1 wherein said error event pattern is $ex =$
2 $\pm\{1-1\}$.

1 7. The method of claim 1 wherein said filtering is accomplished by
2 applying said output to an FIR filter.

1 8. The method of claim 1 further comprising whitening the recovered
2 data output signal, prior to said filtering, with a whitening
3 filter.

1 9. A sampled data detection technique for use in a mass data
2 storage device, comprising:

3 equalizing and sampling a read back signal from a transducer
4 head of said mass data storage device to a partial response level
5 of at least EPR4 to produce an actual sampled partial response
6 target signal;

7 detecting said actual sampled partial response target signal
8 in a Viterbi detector having a partial response detection level of
9 at least EPR4 to produce a recovered data output signal;

10 delaying said actual sampled partial response target signal
11 for a time substantially equal to a time required by said Viterbi
12 detector to generate said recovered data output signal from said
13 actual sampled partial response target signal to produce a delayed
14 actual sampled partial response target signal;

15 converting said recovered data output signal to a partial
16 response level of said actual sampled data output signal to produce
17 a converted recovered partial response target signal;

18 subtracting said converted recovered partial response target
19 signal from said delayed actual sampled partial response target
20 signal to produce an error signal;

21 determining the occurrence of a predetermined error event
22 pattern in said recovered data output signal to produce an error
23 event pattern indicating signal;

24 producing, from said error signal, a detection signal having
25 a magnitude based upon the occurrence of an error event;

26 comparing said detection signal to a predetermined threshold
27 level, and generating an error correction control signal if said
28 data detection signal is larger than said predetermined threshold
29 level, and said error event pattern indicating signal indicates an
30 occurrence of an error pattern; and

31 correcting said recovered data output signal to correspond to
32 said predetermined data pattern if said error correction control
33 signal has been generated.

1 10. The method of claim 9 wherein said equalizing comprises
2 equalizing said read back signal to a partial response level of
3 EPR4, and said detecting comprises detecting said actual sampled
4 partial response target signal in a Viterbi detector having a
5 partial response detection level of EPR4.

1 11. The method of claim 9 wherein said equalizing comprises
2 equalizing said read back signal to a partial response level of
3 EEPR4, and said detecting comprises detecting said actual sampled
4 partial response target signal in a Viterbi detector having a
5 partial response detection level of EEPR4.

1 12. The method of claim 9 wherein said producing a detection signal
2 comprises filtering said error signal with an FIR filter.

1 13. The method of claim 9 further comprising whitening said error
2 signal prior to said producing said detection signal.

1 14. The method of claim 9 wherein said determining the occurrence
2 of a predetermined error event pattern in said recovered data
3 output signal comprises determining the occurrence of $ex = \pm\{1\}$ in
4 said recovered data output signal.

1 15. The method of claim 9 wherein said determining the occurrence
2 of a predetermined error event pattern in said recovered data
3 output signal comprises determining the occurrence of $ex = \pm\{1-11\}$
4 in said recovered data output signal.

1 16. The method of claim 9 wherein said determining the occurrence
2 of a predetermined error event pattern in said recovered data
3 output signal comprises determining the occurrence of $ex = \pm\{1-1\}$
4 in said recovered data output signal.

1 17. The method of claim 9 wherein said determining the occurrence
2 of a predetermined error event pattern in said recovered data
3 output signal comprises determining a data sequence having a high
4 likelihood of occurrence.

1 18. A post-processor circuit for use in a sampled data read channel
2 of a mass data storage device, comprising:

3 a Viterbi detector that receives an actual sampled partial
4 response target signal from a storage medium of said mass data
5 storage device to produce a recovered data output signal;

6 an error pattern detector to generate an error pattern event
7 indicating signal if a predetermined error event pattern occurs in
8 said sampled partial response target signal;

9 a circuit for generating an error signal based upon a
10 difference between said recovered data output signal and a delayed
11 said actual sampled partial response target signal;

12 a threshold circuit to generate an error correction control
13 signal if a magnitude of said error signal exceeds a predetermined
14 threshold;

15 and an error correction circuit to modify the recovered data
16 output signal when said error correction control signal and said
17 error event pattern indicating occurrence signal are generated.

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1 19. The circuit of claim 18 further comprising a whitening filter
2 connected to receive said error signal to produce an input signal
3 to said threshold circuit.

1 20. The circuit of claim 19 wherein said whitening filter has a
2 transfer function, $NW(D)$, that is equal to

3
$$(1+a_1*D+a_2*D^2+\dots+a_n*D^n)/(1+b_1*D+b_2*D^2+\dots+b_m*D^m),$$

4 in which a_1, a_2, \dots, a_n , and b_1, b_2, \dots, b_m are
5 coefficients related to a density in which data is recorded in said
6 mass data storage device.

1 21. The circuit of claim 19 wherein said whitening filter has a
2 transfer function, $NW(D)$, that is equal to

3
$$(1+a_1*D+a_2*D^2+a_3*D^3)/(1+D),$$

4 in which a_1, a_2 , and a_3 are coefficients related to a density in
5 which data is recorded in said mass data storage device.

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1 22. The circuit of claim 18 wherein said predetermined error
2 pattern event is $ex = \pm\{1\}$.

1 23. The circuit of claim 18 wherein said predetermined error
2 pattern event is $ex = \pm\{1-11\}$.

1 24. The circuit of claim 18 wherein said predetermined error
2 pattern event is $ex = \pm\{1-1\}$.

1 25. The circuit of claim 18 wherein said circuit for generating an
2 error signal is an FIR filter

1 26. The circuit of claim 18 wherein said circuit for generating an
2 error signal is an error pattern matched filter.

1 27. The circuit of claim 18 wherein said circuit for generating an
2 error signal comprises a whitening noise generator and an FIR
3 filter connected to receive an output of said whitening noise
4 generator.

1 28. The circuit of claim 18 wherein said Viterbi detector has a
2 partial response level of at least $EPR4$.

1 29. The circuit of claim 18 wherein said Viterbi detector has a
2 partial response level of at least $EEPR4$.